Printed Pages – 4 Roll No. : .....

328356(28)

B. E. (Third Semester) Examination, April-May 2020

(New Scheme)

(Et&T Branch)

DIGITAL LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. All questions carry equal marks. Part (a) of each question is compulsory. Attempt any* ***two*** *question from (b), (c) & (d) part. Assume suitable data wherever necessary.*

Unit-I

1. (a) Define self complementing codes with examples. 2

(b) State and prove De Morgan's theorem. 7

(c) Show that : 7

(i) $AB + A\bar{B}C + B\bar{C} = AC + B\bar{C}$

(ii) $A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$

(d) What is Excess-3 code? Why Excess-3 code is called a self-complementing code. Express 129 to an Excess-3 code. 7

Unit-II

2. (a) What is meant by don't care condition? 2

(b) Given the logic equation

$$f = ABC + B\bar{C}D + \bar{A}BC$$

(i) Make a Truth table

(ii) Simplify using k-map

(iii) Realize f using NAND gates only 7

(c) Simplify the following Boolean function into

(i) Sum-of-Products (SOP) form and

(ii) Product-of-sums (POS) form

and realize if using basic gates

$$f(A, B, C, D) = \sum(0, 1, 2, 5, 8, 9, 10).$$ 7

(d) Using Quine-McClusky (Tabular) method, obtain the minimal expression for.

$$f = \sum m(6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$$ 7

Unit-III

3. (a) What do you mean by combinational ckt? 2

(b) Design a full adder using two half adder and OR gate. 7

(c) Design a 4-bit Gray-to-Binary code converter. 7

(d) Design an Even Parity Bit generator for a 4-bit input. 7

Unit-IV

4. (a) What is a Race Condition. 2

(b) Explain Master-slave flip-flop constructed from two R-s flip-flop. 7

(c) Explain *BCD* ripple counter and draw it logic diagram and timing diagram. 7

(d) Briefly explain the design of sequence delector using Mealy type finite state machine. 7

Unit-V

5. (a) What are the different types of logic families used in digital cuts? 2

   (b) Draw the circuit diagram of CMOS NAND gate and explain the operation. List the main advantages of CMOS gate. 7

   (c) What are the characteristics of ECL family? 7

   (d) Draw the circuit of RTL using NOR gate and explain it. 7